REMARKS

In the outstanding Official Action, Applicants were required to update the status (pending, allowed, etc.) of all patent priority applications in the first line of the specification. In response, the instant specification is herewith amended to update the status of all parent priority applications as indicated. With regard to the status of citations in the specification, it is noted that the single piece of prior art cited in the specification is an issued patent, so that no updating is required.

On the merits, claims 3-4 and 6-9 were deemed to be allowable if placed in independent form, while independent claim 1 and claims 2, 5 and 10 were rejected under 35 USC 102(e) as being anticipated by Andreou et al, for the reasons of record. In response, independent claim 1 and claim 3 are herewith amended in order to more clearly and precisely recite the novel features of the instant invention, and it is respectfully submitted that independent claim 1, as herewith amended, and the remaining claims depending therefrom, are clearly patentably distinguishable over the cited and applied reference for the reasons detailed below.

More particularly, it is respectfully submitted that independent claim 1 is clearly patentably distinguishable over the cited and applied reference for at least two distinct reasons.

First, it is suggested in the Action that the prior art shows a pair of inverters coupled to a pair of adders. Although no adders are specifically shown in the reference, as distinguished from adder components 30 as shown in Fig. 1 and resistors xR and R as shown in Fig. 5, nevertheless it is suggested that the drain node can be read as an adder. Applicants respectfully traverse this interpretation of the reference, and submit that a simple circuit node cannot be construed as an adder. Since claim 3, which more specifically recites the component nature of the adder, has been allowed, it is believed that the Examiner accepts and agrees with Applicants' interpretation, but requires a more specific structural recitation that that recited in original claim 1. Accordingly, claim 1 (and claim 3) have been amended in order to more specifically and precisely recite "adder components", thus clearly distinguishing the specific components as shown in Applicants' Figs. 1 and 5 and described in the instant specification from a mere circuit node or connection point as shown in the prior art.

Second, it is suggested in the Action that the reference shows a bias for the pair of buffers being cross-controlled by the input differential signal for controlling the amplification of the buffers. This recited structure is clearly shown in the instant application, in block diagram form in Fig. 1 by the arrows

connected to the sides of buffer elements 20, and also in Fig. 5, wherein both the bases and emitters of the buffer transistors are coupled to the input signals to control the buffer bias. In the reference, on the contrary, the input signals are coupled only to the gates of the buffer transistors, so that these signals serve only as input signals and not signals to control the bias of the buffer states.

In view of the foregoing, it is respectfully submitted that independent claim 1 and the remaining claims depending therefrom are clearly patentably distinguishable over the cited and applied reference. Accordingly, allowance of the currently-pending claims is respectfully submitted to be justified at the present time, and favorable consideration is earnestly solicited. In view of the amendments and arguments presented herein, the allowable claims have not been placed in independent form at the present time, pending a final determination of the patentability of the remaining claims.

Respectfully submitted,

By _____
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